Group 1

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Lab 0 Report

# Introduction

In this lab, we followed the tutorial which uses the FPGA board to build a simple counter.

# Experience/Problems

## Device ID Not Match

When using “I/O Pin Planning (PlanAhead) – Pre-Synthesis,” we noticed that the pins did not match.

After consulting with the TA, we went into “Design Properties” and changed the Device ID to our device’s ID.

## No “Enable” Pin Mapping

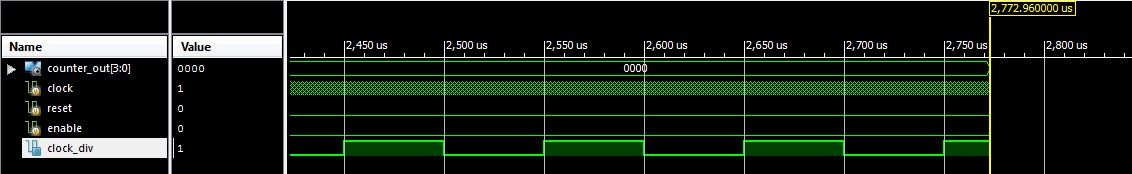
In the tutorial, the input signal “enable” is not mentioned.

We need to manually map the signal enable so that the counter can function properly; without this signal, the counter will not run at all.

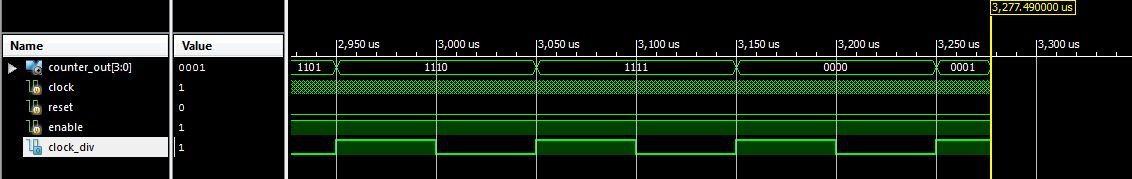
## FPGA Clock Too Fast

The built-in FPGA clock is way too fast for human eyes. When using the built-in clock for the counter, the four LEDs will all light up together. To solve this problem, we made a clock divider.

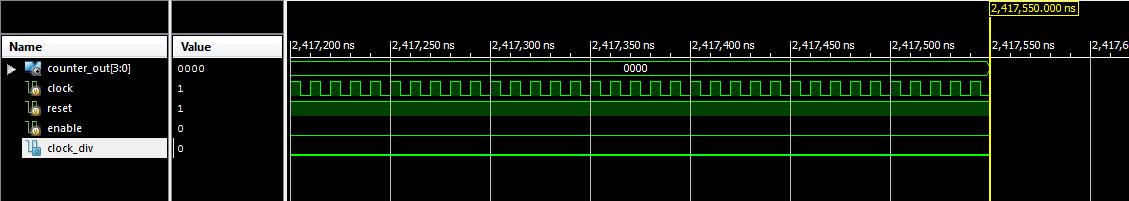
# Waveform Screenshot and Testbench



Both reset and enable are off initially. So, the counter will not start counting until the enable is active.



The enable is active, the counter is incremented by one on each posedge of clock\_div.



As we can see, after reset is pushed, counter\_out[3:0] becomes 0, and then starts counting again.

